REMARKS

This is a full and timely response to the outstanding Action mailed October 5, 2004. Upon entry of the amendments in this response, claims 1 - 31 remain pending. In particular, Applicants have amended claims 1, 14 and 26. Amended claims 1, 14 and 26 further recite the limitation of "having a substantially planar top surface". Support for these amendments can be found at various portions of the application. By way of example, Fig. 2B shows that the blanket dielectric layer 206 is formed overlying the substrate 200, with a substantially planar top surface. Moreover, at page 11, lines 6-20 of the specification, the dielectric layer 206 can be a thick oxide layer with a thickness of about 300-1200Å. That is, the dielectric layer 206 has a sufficient thickness to form a planar top surface. Accordingly, no new matter has been added. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

Rejections under 35 U.S.C. 102

The Office Action indicates that claims 1-10, 12-15, 17-20, 22-26 and 29-31 stand rejected under 35 U.S.C 102(e) as being anticipated by *Furuhata et al* (6,522,587). Applicant respectfully traverses the rejection.

With respect to *Furuhata*, *Furuhata* discloses a non-volatile semiconductor memory device which includes the first voltage-type transistor 100 having a gate insulation layer 20, the second voltage-type transistor 200 having a gate insulation layer 22, and the third voltage-type transistor 300 having a gate insulation layer 24 (Please FIG. 13). In order to fabricate the gate insulation layers 20, 22, and 24 with different thicknesses, a second silicon oxide layer

50bL(24bL) with a thickness of 10-20nm is formed on the surface of the first silicon oxide layer 50aL(24aL) (please see col. 10, lines 3-21 and FIGS. 6-7). Note that the second silicon oxide layer 50bL is conformally formed on the first silicon oxide layer 50aL (please see FIG. 7). That is, the second silicon oxide layer 50bL is a conformal layer and it is impossible to have a planar top surface because the underlying substrate 10 comprising field insulation layers 18 and the first silicon oxide layer 50aL has a non-planar top surface.

Turning now to the amended claims, claim 1 recites:

> 1. A method of forming dielectric layers with various thicknesses on a substrate, comprising the steps of:
>
> providing a first device region and a second device region on the substrate;
>
> growing a first oxide layer on the substrate ;
>
> ***depositing a dielectric layer with a first thickness on the first oxide layer, having a substantially planar top surface***;
>
> removing the dielectric layer and the underlying first oxide layer on the second device region to expose the substrate; and
>
> growing a second oxide layer with a second thickness less than the first thickness on the substrate of the second device region.

(*Emphasis Added*).

Applicant respectfully asserts that *Furuhata* does not teach or otherwise disclose at least certain limitations emphasized above in claim 1. Therefore, Applicant respectfully requests that the rejection of claim 1 be removed and that claim 1 be placed in condition for allowance. Since claims 2 – 9 and 13 are dependent claims that incorporate the limitations of claim 1, and are not otherwise rejected in the Office Action, Applicant respectfully requests that these claims also be placed in condition for allowance.

With respect to claim 14, that claim recites:

> 14. A method of forming gate dielectric layers with various thicknesses on a substrate, comprising the steps of:
>
> providing a first active region and a second active region on the substrate;
>
> forming a first thermal oxide layer on the substrate;
>
> ***depositing a blanket dielectric layer with a first thickness overlying the substrate, having a substantially planar top surface***;
>
> forming a first masking layer overlying the substrate except over the second active region;
>
> etching the dielectric layer and the underlying first thermal oxide layer on the second active region using the first masking layer as an etch mask to expose the substrate;
>
> removing the first masking layer;
>
> forming a second thermal oxide layer with a second thickness less than the first thickness on the second active region; and
>
> forming a first gate on the dielectric layer on the first active region and a second gate on the second thermal oxide layer on the second active region.

(*Emphasis Added*).

Applicant respectfully asserts that *Furuhata* does not teach or otherwise disclose at least certain limitations emphasized above in claim 14. Therefore, Applicant respectfully requests that the rejection of claim 14 be removed and that claim 14 be placed in condition for allowance. Since claims 15, 17 – 20 and 22 - 25 are dependent claims that incorporate the limitations of claim 14, and are not otherwise rejected in the Office Action, Applicant respectfully requests that these claims also be placed in condition for allowance.

With respect to claim 26, that claim recites:

> 26. A method of forming an integrated circuit having gate oxide layers with multiple thicknesses, comprising the steps of:
>
> providing a substrate having a first active region, a second active region, and a third active region;
>
> performing a first oxidation to form a first oxide layer on the substrate;

depositing a blanket high temperature oxide layer with a first thickness overlying the substrate, having a substantially planar top surface;
forming a first photoresist layer on the high temperature oxide layer except over the second active region;
etching the high temperature oxide layer and the underlying first oxide layer on the second active region using the first photoresist layer as an etch mask to expose the substrate;
removing the first photoresist layer;
performing a second oxidation to form a second oxide layer with a second thickness less than the first thickness on the second active region;
forming a second photoresist layer overlying the substrate except over the third active region;
removing the high temperature oxide layer and the underlying first oxide layer on the third active region to expose the substrate;
removing the second photoresist layer;
performing a third oxidation to form a third oxide layer with a third thickness less than the first thickness on the third active region and on the second oxide layer on the second active region; and
forming a first gate on the high temperature oxide layer on the first active region, a second gate on the second oxide layer on the second active region, and a third gate on the third thermal oxide layer on the third active region.

(*Emphasis Added*).

Applicant respectfully asserts that *Furuhata* does not teach or otherwise disclose at least certain limitations emphasized above in claim 26. Therefore, Applicant respectfully requests that the rejection of claim 26 be removed and that claim 26 be placed in condition for allowance. Since claims 29 - 31 are dependent claims that incorporate the limitations of claim 26, and are not otherwise rejected in the Office Action, Applicant respectfully requests that these claims also be placed in condition for allowance.

Rejections under 35 U.S.C. 103

The Office Action indicates that claims 16, 21, and 27 stand rejected under 35 U.S.C 103(a) as being unpatentable over *Furuhata* in view of *Eklund et al.* (US 2003/0096466 A1). Additionally, the Office Action indicates that claims 11 and 28 stand rejected under 35 U.S.C 103(a) as being unpatentable over *Furuhata*. Applicant respectfully traverses the rejection.

In particular, as set forth above, Applicant respectfully asserts that *Furuhata* does not teach or reasonably suggest at least certain limitations that have been emphasized in the respective independent claims. Since *Eklund* also does not teach or reasonably suggest at least these limitations, Applicant respectfully asserts that the rejection of claims 11, 16, 21, 27 and 28 is deficient and that these dependent claims are in condition for allowance.

Cited Art Made of Record

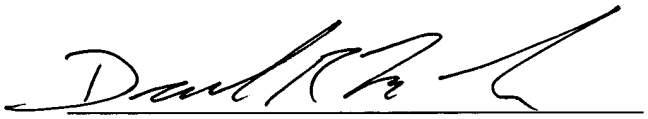
The cited art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed, rendered moot, and/or accommodated, and that the now pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this amendment and response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,



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